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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/738,472	12/17/2003	Chang-Rong Wu	10113491	8197

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/738,472	WU ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on May 27, 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-19, 25, 26, and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (US 6,391,705 B1) in view of Gruening et al. (US 6,184,091 B1).

In re claim 17, Hsiao et al. discloses (figs. 2-10A) a method for fabricating a memory device with a vertical transistor and a trench capacitor, comprising: providing a substrate (200); forming at least one deep trench (302) in the substrate; forming a trench capacitor (504) in the bottom of the deep trench; forming a conducting wire (604 and 702) on the trench capacitor; forming a trench top insulating layer (802) on the conducting wire, and forming a control gate (1104) on the trench top insulating layer. Hsiao shows all of the elements of the claims except the trench top insulating layer consisting of a first insulating layer and a second insulating layer surrounded by the first insulating layer. Gruening et al. discloses a method of forming a memory device comprising the step of forming a top insulating layer (40 in fig. 3) having a first insulating layer (36) and a second insulating layer (44) surrounded by the first insulating layer.

With such a configuration, an improved trench top insulation layer is formed (col. 5, lines 13-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trench top oxide of Hsiao by using a first and second insulating layer as taught by Gruening to form an improved, reliable trench top insulation.

In re claims 18 and 19, Hsiao shows (fig. 12A) the method further comprising a buried strap (704) in the substrate beside the conducting wire to electrically connect the control gate as a drain and a doped area in the substrate beside the control gate as a source (1210).

In re claims 25 and 26, Gruening discloses (col. 4, line 59 – col. 5, line 19) that the first insulating layer is nitride and the second insulating layer is TEOS oxide. Gruening also discloses (col. 5, lines 38-41) that the thickness of the second insulating layer is within the range recited in claim 26.

In re claims 28-31, as far as understood, Hsiao shows (fig. 7) that the conducting wire has a first conducting layer (604) and a second conducting layer (702), the first conducting layer of the conducting wire and the substrate are isolated by a circular insulating layer (602), and the second conducting layer is formed on the first conducting layer and the circular insulating layer. The first conducting layer is a doped poly layer or a doped epi-silicon layer, the second conducting layer is a poly layer or an epi-silicon layer, and the circular insulating layer is a silicon oxide layer (col. 3, line 41 col. 4, line13).

In re claim 32, Hsiao shows (fig. 10A) that the control gate consists of a gate conducting layer (1104) and a gate oxide layer (1002), and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof (col. 5, lines 20-28).

Claims 20-24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (US 6,391,705 B1) in view of Gruening et al. (US 6,184,091 B1) as applied to claim 17 above, and further in view of Nitayama et al. (US 6,720,606 B1).

In re claims 20-24, Hsiao in view of Gruening show all of the elements of the claims except the first insulating layer being and oxide nitride layer. Nitayama et al. discloses (col. 11, lines 25-38) discloses a method of forming an insulator (130) for a trench capacitor. The insulating liner portion comprises about 5nm (50 Angstroms) of oxide and about 5nm (50 Angstroms) of nitride. The oxide is formed by thermal oxidation and the nitride is formed by CVD. Although the references don't disclose the desired range of the oxide layer thickness of the oxide-nitride, it would have been obvious to one of ordinary skill in the art to make the thickness of the oxide within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.* Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the single nitride first insulating layer of Hsiao and Gruening by substituting it with an oxide-nitride

layer as taught by Nitayama to provide a more reliable insulating liner for the trench top insulation.

In re claim 27, Nitayama further discloses (col. 11, lines 25-38) that a subsequent TEOS layer is formed by LPCVD.

Claims 33-35, 41, 42, and 44-47, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (US 6,391,705 B1) in view of Jammy et al. (US 6,222,218 B1) and Gruening et al. (US 6,184,091 B1).

In re claim 33, as far as understood, Hsiao et al. discloses (col. 3, line 42 – col. 5, line 40) and figs. 2-10A) a method for fabricating a memory device with a vertical transistor and a trench capacitor, comprising: providing a substrate (200); forming at least one deep trench (302) in the substrate; forming a trench capacitor (504) in the bottom of the deep trench; forming a insulating layer (602) on the trench capacitor, a sidewall of the deep trench, and the substrate; etching the insulating layer until the insulating layer on the trench capacitor and the substrate is removed to form a circular insulating layer (602) on the sidewall of the deep trench (col. 3, lines 40-55); filling a first conducting layer (604) in the deep trench; etching the first conducting layer to expose the circular insulating layer (col. 3, lines 55-65); forming a second conducting layer (702) on the first conducting layer, the circular insulating layer, the sidewall of the deep trench, and the substrate; partially etching the second conducting layer to remove the second conducting layer on the sidewall of the deep trench and the substrate (col. 4, lines 1-13), in which a conducting wire consists of the first conducting layer and the

second conducting layer; conformably forming a first insulating layer (706) on the second conducting layer, the sidewall of the deep trench, and the substrate; partially etching the first insulating layer to remove the first insulating layer on the second conducting layer and the substrate to form a spacer on the sidewall of the deep trench (col. 4, lines 29-42); filling a second insulating layer (802) in the deep trench; etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating layer; and forming a control gate (1004) on the trench top insulating layer. Hsiao shows all of the elements of the claims except the method of etching the circular insulating layer to below the first conducting layer. Jammy et al. discloses a process (see figs. 3f-3i) of forming a trench capacitor comprising etching the circular insulating layer (30) to below the first conducting layer (32) in the deep trench (col. 8, line 62 – col. 9, line 26). A second conducting layer (34) is formed on the first conducting layer and the circular insulating layer and is then etched to leave the second conducting layer coning the first conducting layer and the circular insulating layer (fig. 3i and col. 9, lines 18-26). With this configuration, the buried strap outdiffusion is limited, thus improving the electrical characteristics of the device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conducting wire of Hsiao by forming the second conducting layer coning the first conducting layer and circular insulating layer as taught by Jammy to limit the outdiffusion of a subsequent buried strap, thus improving the electrical characteristic of the device.

Neither reference discloses the process of forming the trench top insulating layer which includes etching the second insulating layer to expose the first insulating layer and etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating to leave the first insulating layer on a sidewall of the second insulating layer, in which a trench top insulating layer consists of the first insulating layer and the second insulating layer. Gruening et al. discloses (figs. 2-5) a method of forming an improved trench top insulating layer comprising etching a second insulating layer (44) to expose the first insulating layer (36) (col. 5, lines 13-19) and etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating to leave the first insulating layer on a sidewall of the second insulating layer (col. 5, lines 52-67), in which a trench top insulating layer consists of the first insulating layer and the second insulating layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trench top oxide of Hsiao by forming and etching a first and second insulating layer as taught by Gruening to form an improved, reliable trench top insulation.

In re claims 34 and 35, Hsiao shows (fig. 12A) the method further comprising a buried strap (704) in the substrate beside the conducting wire to electrically connect the control gate as a drain and a doped area in the substrate beside the control gate as a source (1210).

In re claims 41 and 42, Gruening discloses (col. 4, line 59 – col. 5, line 19) that the first insulating layer is nitride and the second insulating layer is TEOS oxide.

Gruening also discloses (col. 5, lines 38-41) that the thickness of the second insulating layer is within the range recited in claim 42.

In re claims 44-46, Hsiao discloses that the first conducting layer is a doped poly layer or a doped epi-silicon layer, the second conducting layer is a poly layer or an epi-silicon layer, and the circular insulating layer is a silicon oxide layer (col. 3, line 41 col. 4, line13).

In re claim 47, Hsiao shows (fig. 10A) that the control gate consists of a gate conducting layer (1104) and a gate oxide layer (1002), and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof (col. 5, lines 20-28).

Claims 36-40 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (US 6,391,705 B1) in view of Jammy et al. (US 6,222,218 B1) and Gruening et al. (US 6,184,091 B1) as applied to claim 33 above, and further in view of Nitayama et al. (US 6,720,606 B1).

In re claims 36-40, Hsiao in view of Jammy and Gruening show all of the elements of the claims except the first insulating layer being and oxide nitride layer. Nitayama et al. discloses (col. 11, lines 25-38) discloses a method of forming an insulator (130) for a trench capacitor. The insulating liner portion comprises about 5nm (50 Angstroms) of oxide and about 5nm (50 Angstroms) of nitride. The oxide is formed by thermal oxidation and the nitride is formed by CVD. Although the references don't disclose the desired range of the oxide layer thickness of the oxide-nitride, it would have

been obvious to one of ordinary skill in the art to make the thickness of the oxide within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.* Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the single nitride first insulating layer of Hsiao, Jammy, and Gruening by substituting it with an oxide-nitride layer as taught by Nitayama to provide a more reliable insulating liner for the trench top insulation.

In re claim 43, Nitayama further discloses (col. 11, lines 25-38) that a subsequent TEOS layer is formed by LPCVD.

Response to Arguments

Applicant's arguments filed with respect to claims 17-47 have been fully considered but they are not persuasive. The applicant primarily asserts that the prior art references do not show all of the elements of the claims, specifically that Gruening et al. does not cure the deficiencies of Hsiao et al. because the nitride layer (36) of Gruening is stripped from the trench sidewall. The examiner believes that the cited references show all of the elements of the claims. As stated in the rejection above, Hsiao et al. shows all of the elements of the claims except the trench top insulating layer consisting of a first insulating layer and a second insulating layer surrounded by the first insulating layer. Gruening was cited to cure that deficiency. Although Gruening states that the sidewall insulation layer (36) is stripped from the sidewall of the trench, Gruening does

not specifically state that the portion of the sidewall insulation layer (36) adjacent and surrounding the trench top isolation layer (44) is stripped. In figure 5 of Gruening, the dark portions of trench top isolation layer (44) pertain to the remaining portions of the sidewall insulation layer (36), thus being a second insulating layer surrounding the first insulating layer. If the sidewall insulation layer (36) were completely stripped even in the portions surrounding the trench top isolation layer (44), then trench top isolation layer would cease to completely isolate the lower capacitor from the conductor (56) located above. Thus one of ordinary skill in the art would look to Gruening for a trench top insulating layer consisting of a first insulating layer and a second insulating layer surrounded by the first insulating layer to form an improved, reliable trench top insulation layer. Therefore, the cited references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

August 4, 2005

TOM THOMAS
SUPERVISORY PATENT EXAMINER